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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

1 of 2

Complete if Known

Application/Cnf. No.	10/084,569	/	7959
Filing Date	February 27, 2002		
First Named Inventor	Ahmad R. Ansari		
Art Unit	2185		
Examiner Name	Unknown		
Attorney Docket Number	X-987 US		

U.S. PATENT DOCUMENTS

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¹ Applicant's unique citation designation number (optional). ² See Kinds of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Sheet 2 of 2

OTHER – NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No'	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 2
<i>JM</i>		Cary D. Snyder and Max Baron; "Xilinx's A-to-Z System Platform"; Cahners Microprocessor; The Insider's Guide to Microprocessor Hardware; Microdesign Resources; February 6, 2001; pp. 1-5.	
		</td	

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Subscribed and sworn to before me on 1449A/PTO				Applicant / Conf. N.	10/084,569 / 7959
				Filing Date	February 27, 2002
				First Named Inventor	Ahmad R. Ansari
				Art Unit	2185
				Examiner Name	Unknown
Sheet	1	of	7	Attorney Docket Number	X-987 US

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First Named Inventor	Ahmad R. Ansari		
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Attorney Docket Number	X-987 LIS		

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. *	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
		US- 4,758,985	07-19-88	Carter	
		US- 5,142,625	08-25-92	Nakai	
		US- 4,855,669	08-08-89	Mahoney	
		US- 34,363	08-31-93	Freeman	
		US- 5,072,418	12-10-91	Boutaud et al.	
		US- 5,274,570	12-28-93	Izumi et al.	
		US- 5,550,782	08-27-96	Cliff et al.	JAN 2 2 2004
		US- 5,347,181	09-13-94	Ashby et al.	
		US- 5,339,262	08-16-94	Rostoker et al.	
		US- 5,311,114	05-10-94	Sambamurthy et al.	
		US- 5,504,738	04-02-96	Sambamurthy et al.	
		US- 5,552,722	09-03-96	Kean	
		US- 5,361,373	11-01-94	Gilson	
		US- 5,537,601	07-16-96	Kimura et al.	
		US- 5,457,410	10-10-95	Ting	
		US- 5,740,404	04-14-98	Baji	
		US- 5,581,745	12-03-96	Muraoka	
		US- 5,742,179	04-21-98	Sasaki	
		US- 5,600,845	02-04-97	Gilson	
		US- 5,574,930	11-12-96	Halverson Jr., et al.	

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OTHER - NON PATENT LITERATURE DOCUMENTS

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		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINI, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		JACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		P.C. FRENCH et al., "A SELF-RECONFIGURING PROCESSOR," IEEE, July 1993, pp. 50-59, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		ANDRE' DEHON, "DPGA-COUPLED MICROPROCESSORS: COMMODITY ICs FOR THE EARLY 21ST CENTURY," IEEE, February 1994, pp. 31 - 39, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

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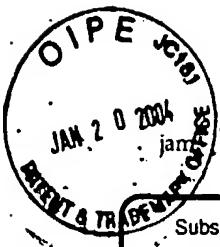
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Sheet 3 of 7

Substitute for form 1449A/PTO				Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application / Case No.	10/084,569 / 7959	
(use as many sheets as necessary)				Filing Date	February 27, 2002	
				First Named Inventor	Ahmad R. Ansari	
				Art Unit	2185	
				Examiner Name	Unknown	
Sheet	3	of	7	Attorney Docket Number		
X-987 US						

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code (if known)			
MM		US- 5,473,267	12-05-95	Stansfield	
MM		US- 5,742,180	04-21-98	DeHon et al.	
BB		US- 5,737,631	04-07-98	Trimberger	
MM		US- 5,748,979	05-05-98	Trimberger	
MM		US- 5,752,035	05-12-98	Trimberger	
MM		US- 6,026,481	02-15-00	New et al.	RECEIVED
MM		US- 5,705,938	01-06-98	Kean	
MM		US- 5,500,943	03-19-96	Ho et al.	JAN 22 2004
MM		US- 5,652,904	07-29-97	Trimberger	
MM		US- 5,809,517	09-15-98	Shimura	Technology Center 2100
MM		US- 5,543,640	08-06-96	Sutherland et al.	
MM		US- 5,574,942	11-12-96	Colwell et al.	
MM		US- 6,604,228	08-05-03	Patel et al.	
MM		US- 5,933,023	08-03-99	Young	
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MM		US- 6,389,558	05-14-02	Herrmann et al.	
MM		US- 5,732,250	03-24-98	Bates et al.	
MM		US- 5,889,788	03-30-99	Pressly et al.	
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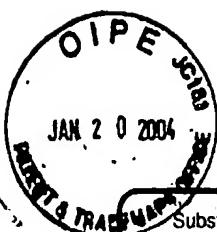
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Application/Cnf. N.	10/084,569	/	7959
Filing Date	February 27, 2002		
First Named Inventor	Ahmad R. Ansari		
Art Unit	2185		
Examiner Name	Unknown		
Attorney Docket Number	X-987 US		

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		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-9 to 2-18; 2-187 to 2-199, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		CHRISTIAN ISELI et al., "AC++ COMPILER FOR FPGA CUSTOM EXECUTION UNITS SYNTHESIS," 1995, pp. 173-179, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		INTERNATIONAL BUSINESS MACHINES, "POWERPC 405 EMBEDDED PROCESSOR CORE USER MANUAL," 1996, 5TH Ed., pp. 1-1 TO X-16, International Business Machines, 1580 Rout 52, Bldg. 504, Hopewell Junction, NY 12533-6531.	
		YAMIN LI et al., "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," January 27, 1999, Ch. 3, pp 3-1 TO 3-50, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
		WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

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Signature*John C. Cho*Date
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		Number - Kind Code (if known)	MM-DD-YYYY		
MM		US- 6,011,407	01-04-00	New	
MM		US- 6,172,990	01-09-01	Deb et al.	
MM		US- 5,970,254	10-19-99	Cooke et al.	
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MM		US- 6,211,697	04-03-01	Lien et al.	
MM		US- 6,163,166	12-19-00	Bielby et al.	
MM		US- 6,272,451	08-07-01	Mason et al.	

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MM		US- 6,434,735	08-13-02	Watkins	
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